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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/584,395	06/23/2006	Keiko Fukuda	XA-10578	9000

181 7590 02/04/2008

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EXAMINER	
COLE, BRANDON S	

ART UNIT	PAPER NUMBER
4125	

NOTIFICATION DATE	DELIVERY MODE
02/04/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/584,395	FUKUDA ET AL.	
	Examiner	Art Unit	
	BRANDON S. COLE	4125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-12 and 15-18* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/23/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Paragraph [0010] says that Q1 is set to a value which is n times as large as an emitter current density of the transistor Q2 but fails to show this in the drawings. Instead the drawing shows that Q2 is n times (xn) as larger as Q1. Appropriate correction is required.

Claim Objections

1. Claim 3 objected to because of the following informalities: it says that the emitter area of the first transistor is set larger than an emitter area of the second transistor but fails to show this in the drawings. Instead the drawing shows that the second resistor is n times (xn) larger than the first resistor. It is believed that the applicant meant that the second transistor is supposed to be the transistor with the larger emitter area. Appropriate correction is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1-3 and 5-18 rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al (US 2006/0220634).

As to claim 1, Ito et al figure 4 shows a voltage generating circuit comprising: a first transistor (npn1) which allows a first current (Ie2) to flow in an emitter thereof; a second transistor (npn0) which allows a second current (Ie1) which has a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof (taught in paragraph [0006]); a first resistance (R3) which is provided between the emitter of the first transistor and the emitter of the second transistor; a second resistance (R4) which is provided between the emitter of the second transistor and a ground potential (gnd) of the circuit; a third resistance (R2) which is provided between a collector of the first transistor and a power source voltage (Vext); a fourth resistance (R1) which is provided between a collector of the second transistor and the power source voltage (Vext); and a differential amplifier circuit (Ampnd) having the CMOS constitution which forms an output voltage (Vbgr) upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor and, at the same time, supplies the output voltage to bases of the first transistor and the second transistor in common, whereinthe first transistor (NPN TRANSISTOR) and the second transistor (NPN TRANSISTOR) are constituted by making use of a semiconductor region (figure 22) formed in a process of a CMOS circuit which constitutes the differential amplifier circuit (NMOS TRANSISTOR AND PMOS TRANSISTOR).

As to claim 2, Ito et al figure 4 shows a voltage generating circuit wherein the third resistance (R2) and the fourth resistance (R1) are configured to possess a same resistance value. Ito et al teaches in paragraph [0035] that resistors R1 and R2 have the same resistance

As to claim 3, Ito et al figure 4 shows a voltage generating circuit wherein the emitter area of the first transistor (npn1) is set larger than an emitter area of the second transistor (npn0). (of areas or a number equivalent to m times (1:m).)

Claim 5 recites similar limitations as to claim 1, therefore the claim is rejected for the same reasons.

As to claim 6, Ito et al figure 22 shows a CMOS circuit which is constituted of a second conductive-type well region (NW) and a first conductive-type well region (PW) which are formed on a first conductive-type semiconductor substrate (PSUB), a first conductive-type MOSFET (PMOS TRANSISTOR) which is formed on the second conductive-type well region, and a second conductive-type MOSFET (NMOS TRANSISTOR) which is formed on the first conductive-type well region, and the first transistor and the second transistor which constitute the reference voltage generating circuit are formed of a bipolar transistor (npn TRANSISTOR) having the lateral structure which uses diffusion layers (DNW) which are formed in a step for forming source and

drain diffusion layers of the second conductive-type MOSFET which constitutes the CMOS circuit as the collector and the emitter and is operated using the first conductive-type well region on which the diffusion layers which constitute the collector and the emitter are formed as a base.

Claims 7 and 8 are similar to claim 6 therefore the claims are rejected for the same reasons.

As to claim 9, Ito et al figure 22 shows a semiconductor integrated circuit device wherein the first-conductive type is a p-type (PMOS TRANSISTOR) and the second-conductive type is an n-type (NMOS TRANSISTOR), and a power source voltage (gnd) which is supplied from the external terminal is a positive power source voltage.

As to claim 10, Ito et al figure 4 shows a semiconductor integrated circuit device wherein a second transistor (npn0) that is constituted of one transistor and the first transistor (npn1) is constituted by connecting a plurality of unit transistors (npn1....npnm) corresponding to the second transistor in parallel.

As to claim 11 Ito et al figure 4 shows a semiconductor integrated circuit device wherein the first transistor (npn1) is configured such that the plurality of unit transistors are formed on the well regions having the same depth, and one of the plurality of unit transistors which are formed to have the same constitution as the first transistor is used

as the second transistor. Ito et al teaches in paragraph [0033] that the transistors npn0 and npn1 through npnm are constituted of transistors identical in size to one another and npn1 through npnm are connected in parallel. And unit transistors npn1 through npnm constitute a first transistor and npn0 is the second resistor.

As to claim 12, Ito et al figure 11 shows that the semiconductor integrated circuit device further includes; a power source circuit (REG) which generates an internal voltage (Vint) different from a power source voltage which is supplied from the external terminal upon receiving a reference voltage (Vref) formed by the reference voltage generating circuit (VREFBUF); an internal circuit (CPU) which is operated by the power source circuit; an input circuit (I/O) which is operated upon receiving a power source voltage supplied from the external terminal, performs a level conversion upon receiving an input signal supplied from an external terminal and transmits the signal to the internal circuit; and an output (I/O) circuit which is operated upon receiving a power source voltage supplied from the external terminal, performs a level conversion upon receiving a signal generated by the internal circuit, and forms an output signal to be outputted from the external terminal, wherein the differential amplifier circuit Amppd (figure 17, and figure 18, taught in paragraph [0065] and [0066]) is constituted of a P-channel MOSFET (pm100, figure 17) and an N-channel MOSFET (nm300, figure18) which are formed in the same process as MOSFETs which constitute the input circuit (nm100 and nm110 of figure 17 and pm300 and pm310 of figure18) and the output circuit (out) which

are operated upon receiving a power source voltage supplied from the external terminal (Vext).

As to claim 13, Ito et al figure 11 shows that the semiconductor integrated circuit wherein, the internal voltage (Vint) is formed by reducing the power source voltage supplied from the external terminal (taught in paragraph [0063], and the internal circuit (CPU) is formed withy a minimum forming size of a CMOS processing. It would be obvious for someone having ordinary skill in the art at the time of the invention to create a CPU with the smallest size so that the invention can be used in more applications.

Claims 15 and 16 have similar limitations as to claim 6 therefore, the claims are rejected for the same reasons.

Claims 17 and 18 have similar limitations as to claim 10 therefore, the claims are rejected for the same reasons.

Allowable Subject Matter

4. Claim 14 isobjected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is (571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brandon S Cole/
Examiner, Art Unit 4125

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 4125